Hall Ticket Number:

## VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD B.E. (E.E.E.) II Year II-Semester Advanced Supplementary Examinations, June/July-2017

## **Digital Electronics and Logic Design**

Time: 3 hours

Max. Marks: 70

Code No.: 22214 AS

Note: Answer ALL questions in Part-A and any FIVE from Part-B

Part-A  $(10 \times 2 = 20 \text{ Marks})$ 

1. Implement two input XOR gate using NOR gates only.

2. Simplify the Boolean expression,  $x^{1}yz + x^{1}yz^{1} + xy^{1}z^{1} + xy^{1}z$ .

3. Briefly explain the characteristics of digital IC's.

4. Explain the function of a decoder.

5. Differentiate between serial adder and parallel adder.

6. Solve the following arithmetic sum in Excess-3. ii) 2374+9435

i) 3453+2568

7. Briefly explain about the latch circuit.

8. What is a ring counter?

9. State the differences between a truth table and a state table.

10. List the applications of registers.

## Part-B (5 X 10 = 50 Marks) (All bits carry equal marks)

11. a) Minimize the function using Karnaugh-Map and obtain minimal SOP and POS function.  $f(A, B, C, D) = \pi (1, 2, 3, 8, 9, 10, 11, 14) + \Sigma d (7, 15).$ 

b) Determine canonical POS form for the function  $T(x, y, z) = x(\overline{y} + z)$ .

12. a) Explain the TTL logic family with a neat diagram.

- b) Explain how a decoder can be converted in to a Demultiplexer with relevant block diagrams and truth tables.
- 13. a) Design a full subtractor by using two half subtractors.
  - b) Design a combinational circuit for a 4-bit magnitude comparator.
- 14. a) Draw the schematic circuit of S-R-Flip-Flop with negative edge triggering using NAND gates and explain its operation with proper truth-table. Convert this flip-flop to J-K flipflop and explain its operation.
  - b) Design a synchronous counter using T flip flop for the given sequence  $F = \Sigma (0, 2, 5, 3, 6, 4)$
- 15. a) Bring out the differences among a PAL and PLA.
  - b) Explain the concept of state and state diagram in the design of counters and also draw a state diagram for the given sequence of 10101.
- 16. a) Design a combinational circuit and draw a block diagram for a 4 x 16 decoder constructed with two 3 x 8 decoders.

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- b) Express the following functions in sum of min terms and product of max terms i) F(x, y, z) = (xy + z)(y + xz)ii) F(x, y, z) = 1
- 17. Write short notes on any two of the following:
  - a) Shift register
  - b) BCD arithmetic
  - c) Sequence Detectors